



# AMAZING WORKS HERE

## INTEL CHINA CAMPUS RECRUITING

### 荟萃非凡人才，渴求更多菁英 英特尔大连2020校园招聘火热进行中！



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**目标群体：**2020届或往届硕士及博士毕业生

**目标专业：**化学，物理，材料，计算机、软件、通信、电子、机械、自动化等理工类专业

**工作地点：**大连

**校招官网：**[chinacampus.jobs.intel.com](http://chinacampus.jobs.intel.com)

职位详情、宣讲行程等更多信息登录官网查看，请携带**纸质**简历参加宣讲！

**宣讲安排：**浙江大学（玉泉校区）

校园宣讲	18:30-20:00	10/12/2019 (周六)	永谦活动中心第一报告厅
现场面试	9:00-18:00	10/13/2019 (周日)	就业办面试场地

### 关于英特尔大连-DMTM

DMTM—英特尔全球的第一个存储器芯片工厂，坐落在美丽的海滨城市大连。作为英特尔全球最先进的存储器生产基地，DMTM的拳头产品是英特尔第一代 3D NAND 芯片。英特尔有着长期增长的愿景，而内存和存储将为这个愿景的实现带来强劲的动力，所以DMTM的工作对于英特尔的成功至关重要。简言之，这里销售的每一块内存芯片，都将促进物联网，数据中心和CPU 相关领域的发展—这些正是英特尔的核心增长领域。因此，内存技术作为一项基础技术，对我们支撑智能互联的世界至关重要。

### Intel China Technology Development is Hiring

We are looking for engineers at ALL levels that are excited to be part of one of Intel's fast growing business unit, NSG Non-Volatile Memory Solutions Group. Leveraging success of 3D NAND high volume manufacturing facility, we are ramping up Dalian Technology Development (TD) organization. Join us and help us create the next generation memory technology that serves world's explosive growth of data storage needs and challenges.

#### Position 1- Intel Technology Development Process Engineer

This job requisition is look for multiple candidates for the positions of Process Engineer, reporting to TD Module Engineering Managers. The selected candidates will be responsible for activities covering process, equipment, materials, and operations in their respective areas of expertise, such as CVD/PVD/CMP/Diffusion/Implant/Metro/Lithography/Wet Etch/Dry Etch.

#### Position 2- Intel Technology Development Yield and Integration Engineer

This job requisition is look for multiple candidates for the positions of Yield Engineer, FA Engineer, Defect Reduction Engineer, Integration Engineer, Device Engineer, Quality and Reliability Engineer, and Test Engineer, reporting to TD Integration or Device Engineering Managers.

#### ✓ Mainly Responsibility

Examples of scope of work include silicon process improvement and product enhancement, device capability evaluation and expansion, and wafer cost reduction.

Candidates must have demonstrated a track record of excellence in creative problem solving, device or test capability enabling, or manufacturing process optimization in a relevant engineering organization.

Responsibilities include:

Perform feasibility study and provide integrated process solutions to meet desired device specification and process improvement requirements

Lead new device experimentation, implementation and high volume manufacturing readiness in the area of expertise

Define, explore and qualify new integrated process solutions to meet quality and output needs of new processes for high volume manufacturing ramp.

#### ✓ Qualifications

-- PhD in a science or engineering field and with graduation date in 2020 or recent year before

-- Direct experience in semiconductor research/fabrication environment is highly desired

--Demonstrated technical leadership and a track record of problem solving with creativity and out-of-box thinking

--Strong expertise of process characterization, qualification and troubleshooting is required;

--Motivated self-starter, with strong ability to work independently as well as in a team environment;

--Strong verbal and written communication skills in English;

--Think and operate independently, while simultaneously focusing on many diverse priorities.

--Flexibility and maturity in facing uncertainties and changing priorities/responsibilities

--Commit to aggressive goals and win with a can-do attitude

--Act with velocity and a strong sense of urgency

--Respect cultural diversity and sensitivity

--Agility in learning, improving, and innovating